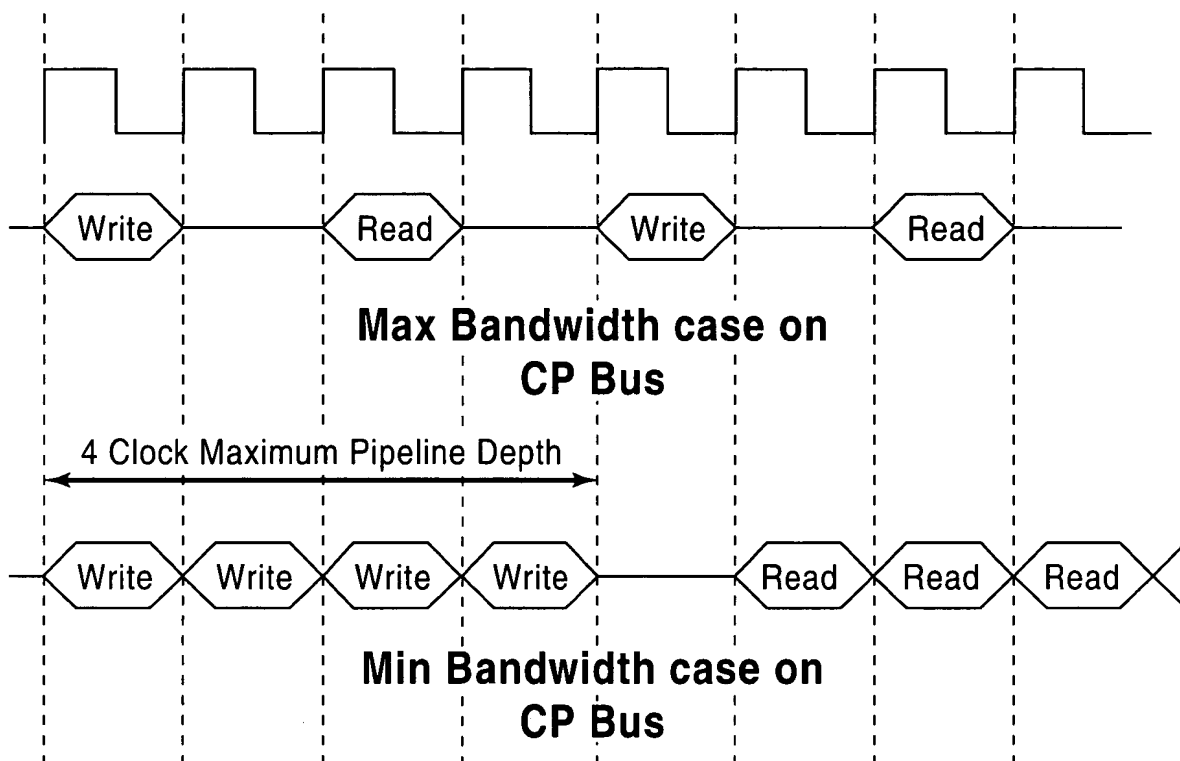


Fig.20



Fig.21





SFAP To SDRAM Scheduler Interface Timings

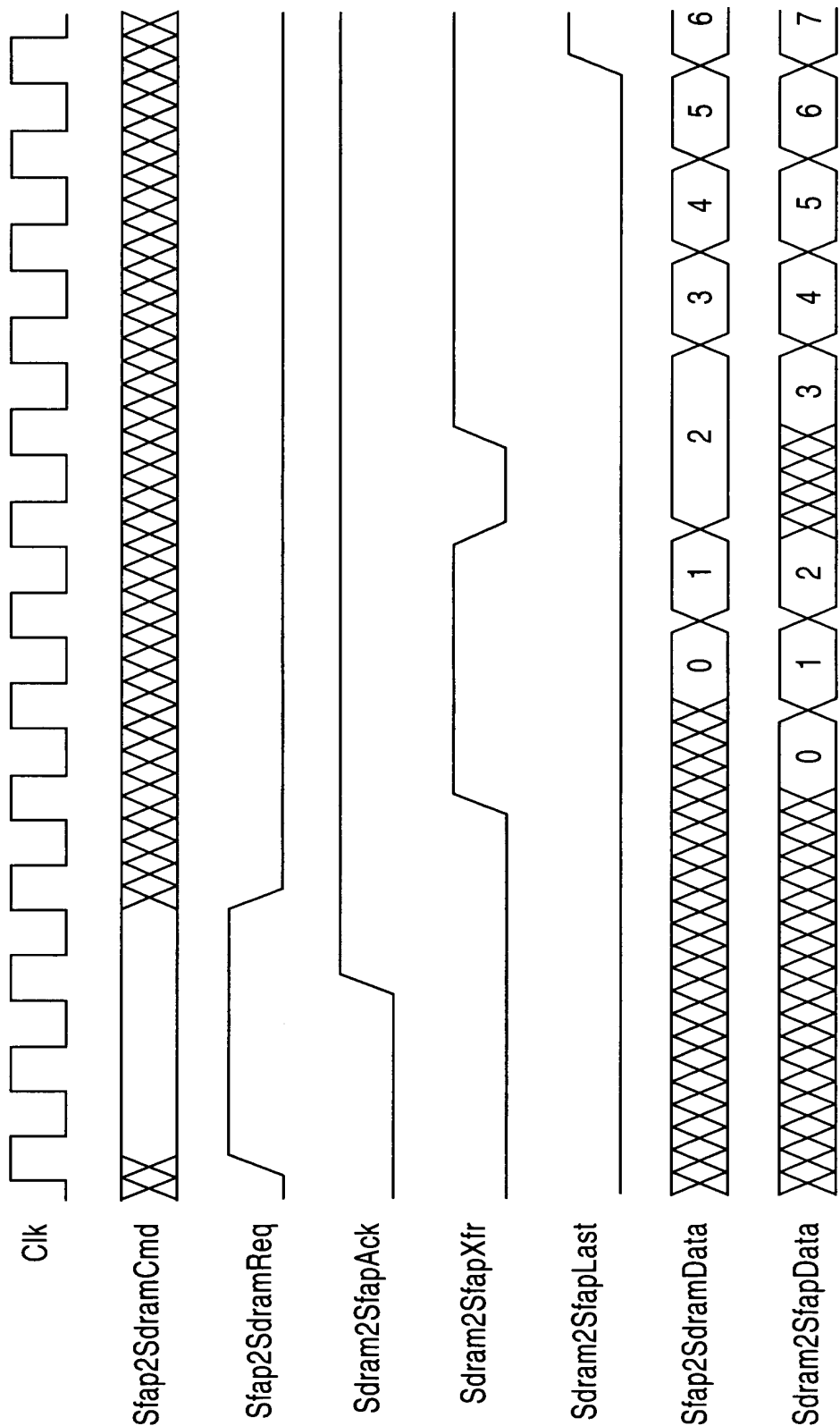


Fig.22



SAU to SDRAM Scheduler Data Transfer

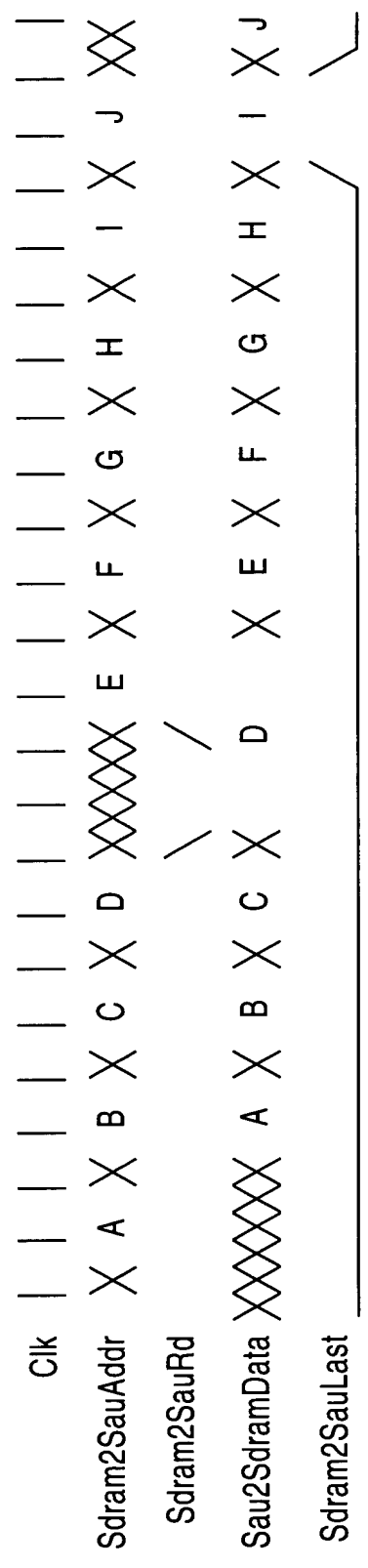


Fig.23



SDRAM Scheduler to SDU Data Transfer

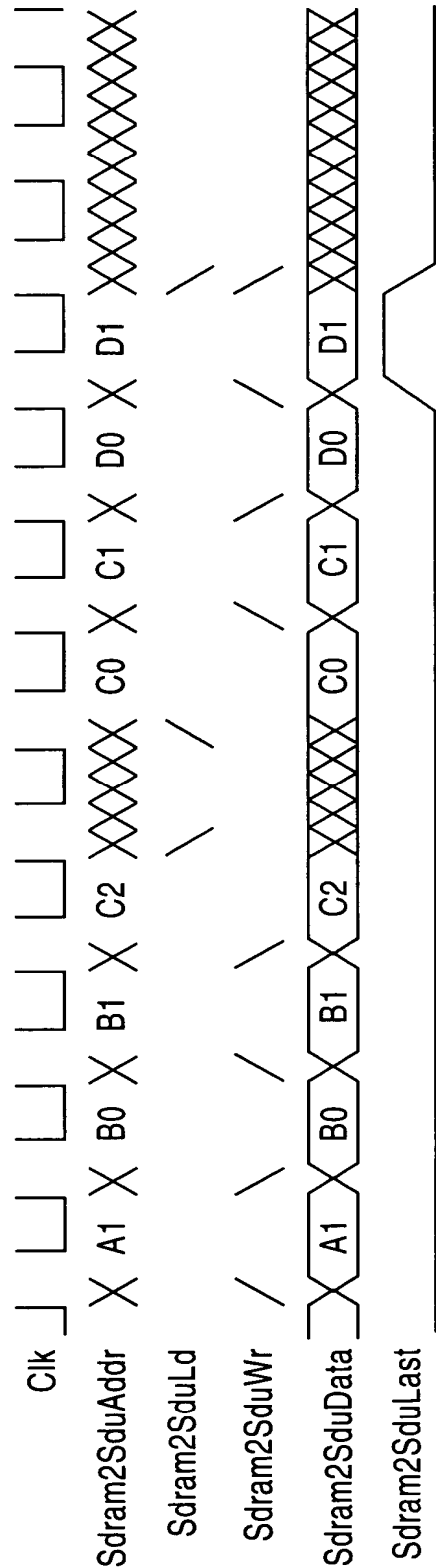


Fig.24



Fig.25

SDRAM Controller Interface Timing

SDRAM Controller Command Input FIFO

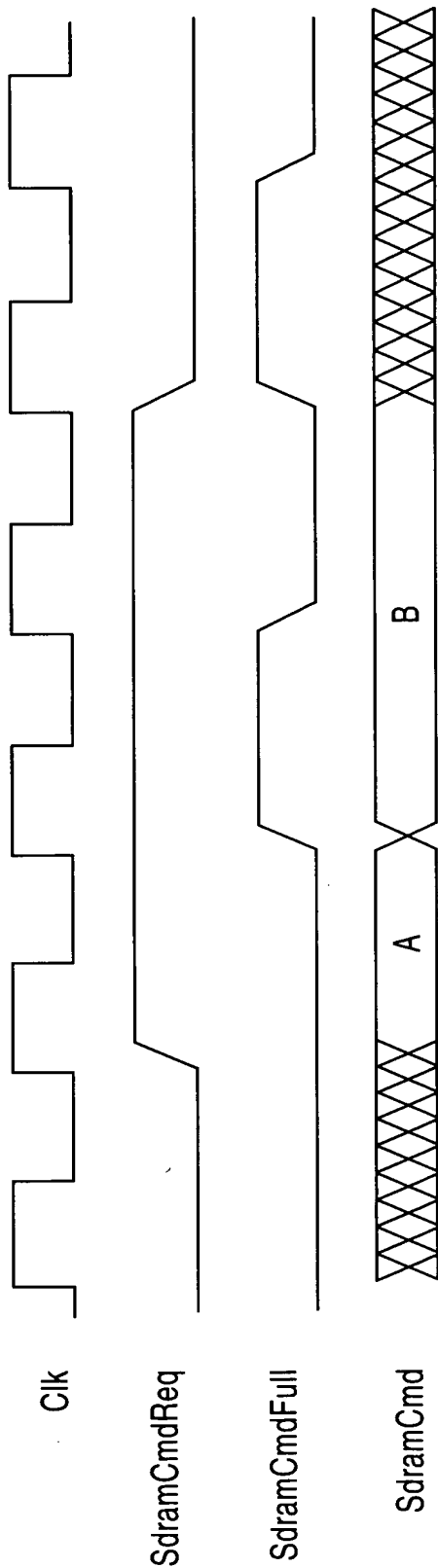




Fig.26

SDRAM Controller Data Write FIFO

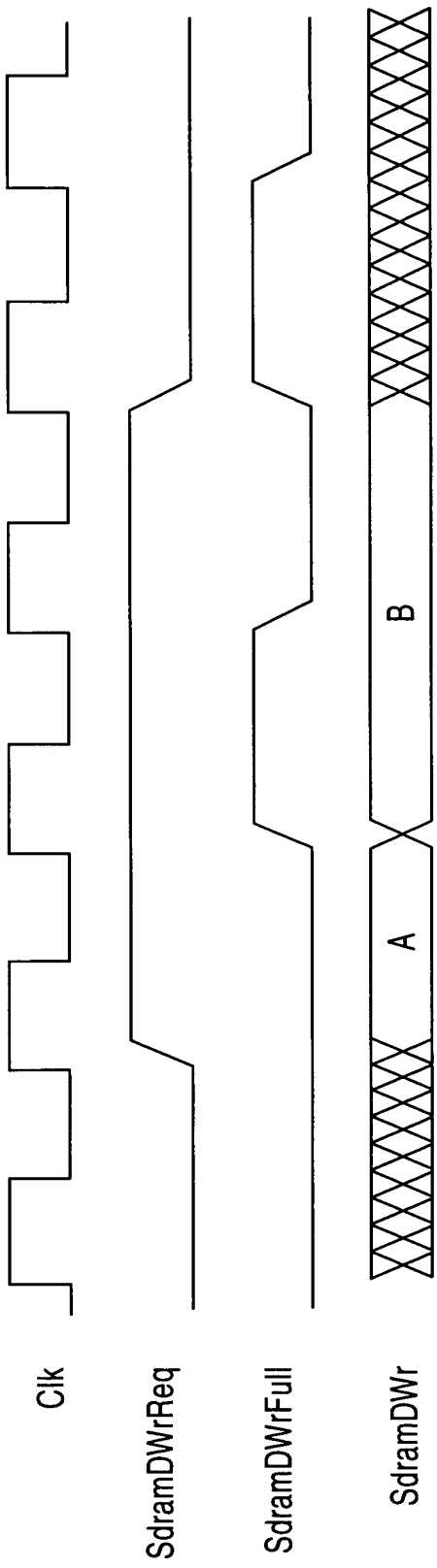
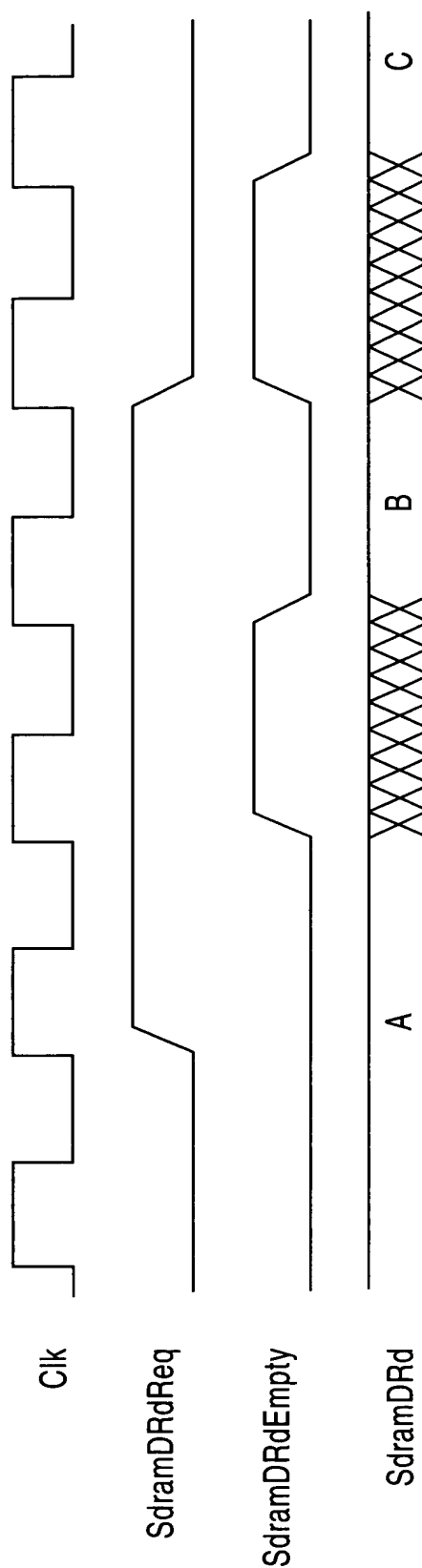
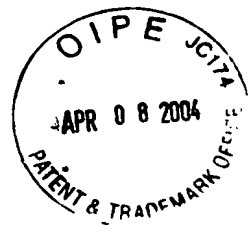


Fig.27

SDRAM Controller Data Read FIFO





Field	Left	Right	Bits
Src	310	306	5
CPUOpcode	305	302	4
BC/MC Bitmap	301	270	32
Cos	269	267	3
P	266	266	1
FC (S)	265	265	1
LC(E)	264	264	1
CRC	263	262	2
Len (0=64)	261	256	6
O	255	254	2
BC/MC	253	253	1
Copy Count (0=32)	252	248	5
Untagged Bitmap	247	216	32
IP	215	215	1
IPX	214	214	1
Time Stamp	213	200	14
Cell Data Bytes 24-0	199	0	200
Total			311

Fig.28

Cell Size	SAU Words	SDRAM Words
00	1	2
01	1	3
10	2	4
11	2	5

Fig.29



Field	Left	Right	Bits	First Only
Last Slot	313	313	1	X
Next Slot ID	312	297	16	X
Copy Count	296	292	5	X
CPUOpcode	291	288	4	
Cell Size	287	286	2	
P	285	285	1	
FC	284	284	1	
LC	283	283	1	
CRC	282	281	2	
Len	280	275	6	
O	274	273	2	
BC/MC	272	272	1	
IP	271	271	1	
IPX	270	270	1	
Time Stamp	269	256	14	

Fig.30

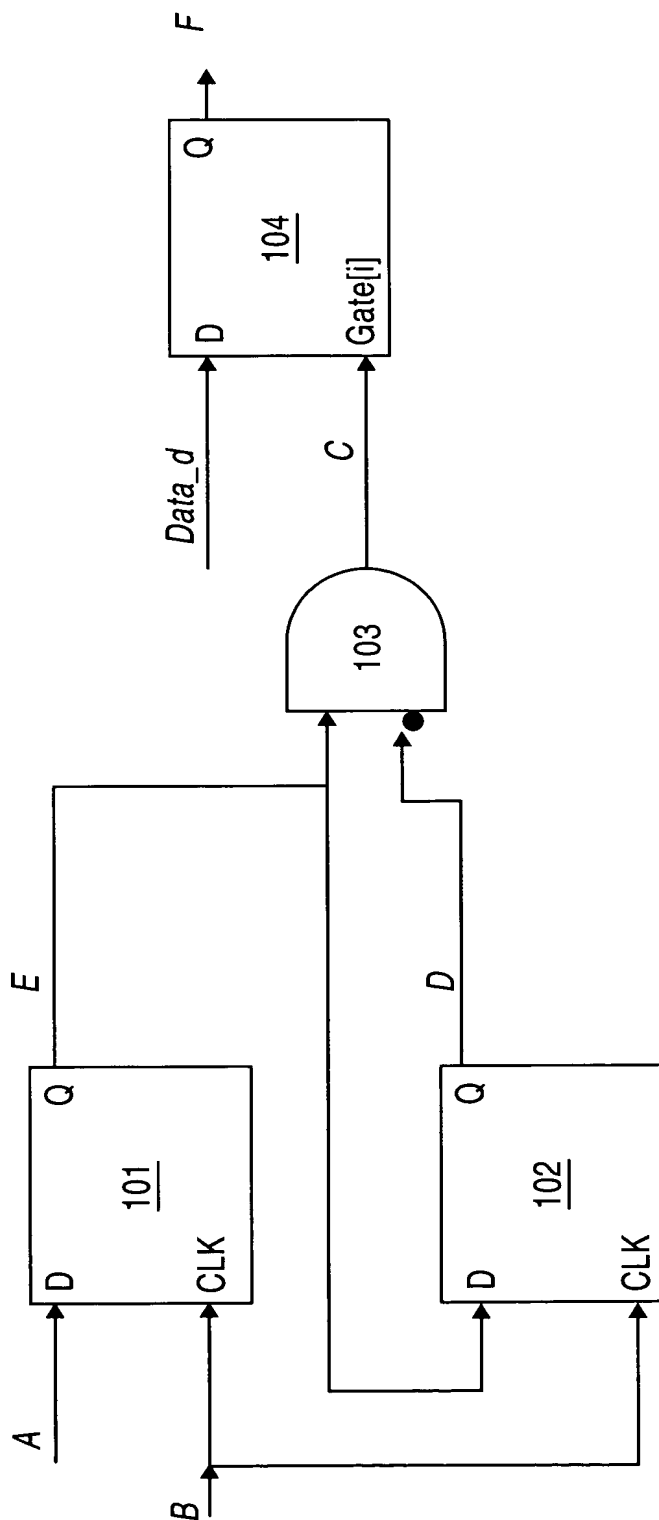
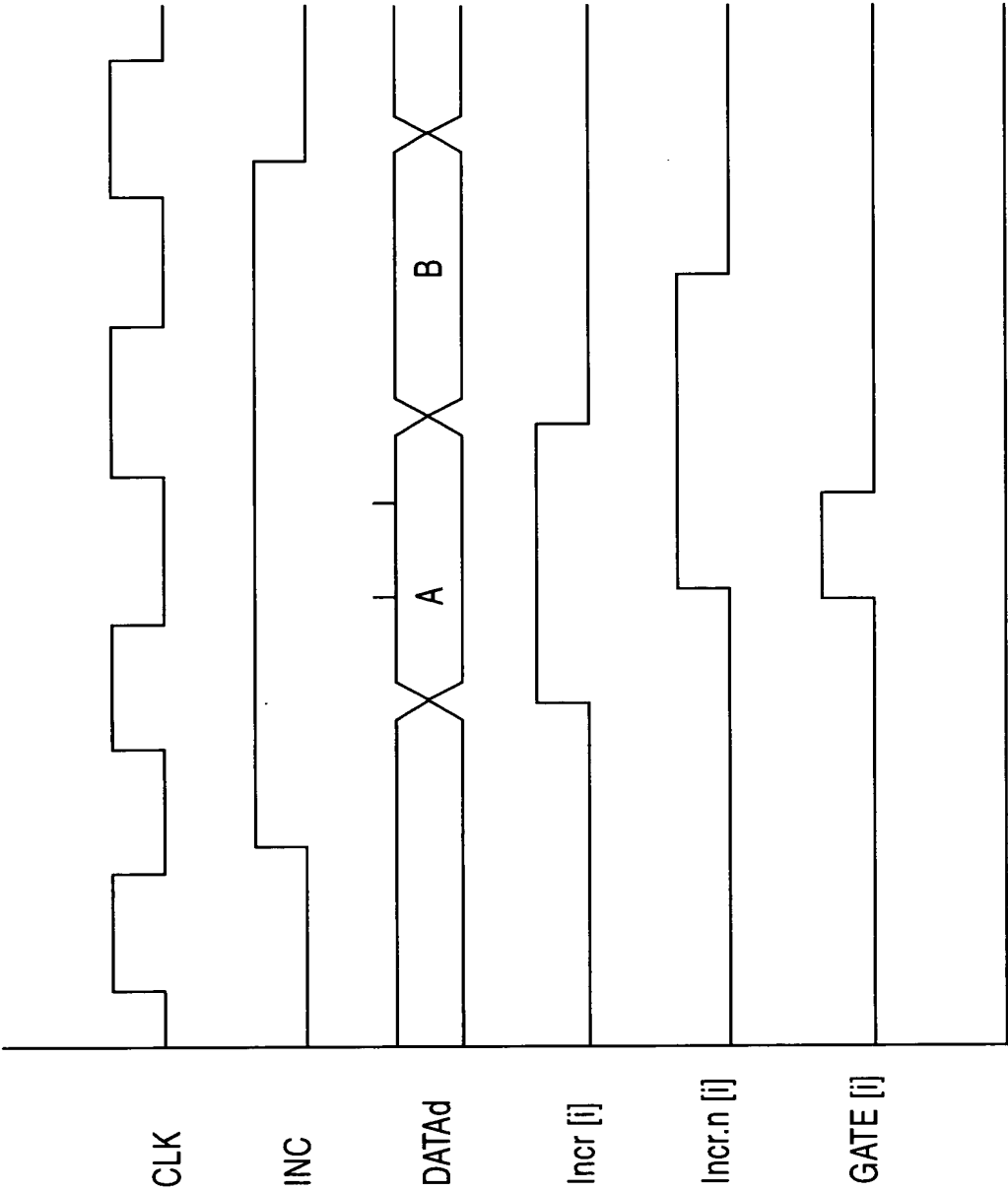


Fig.31



Fig.32



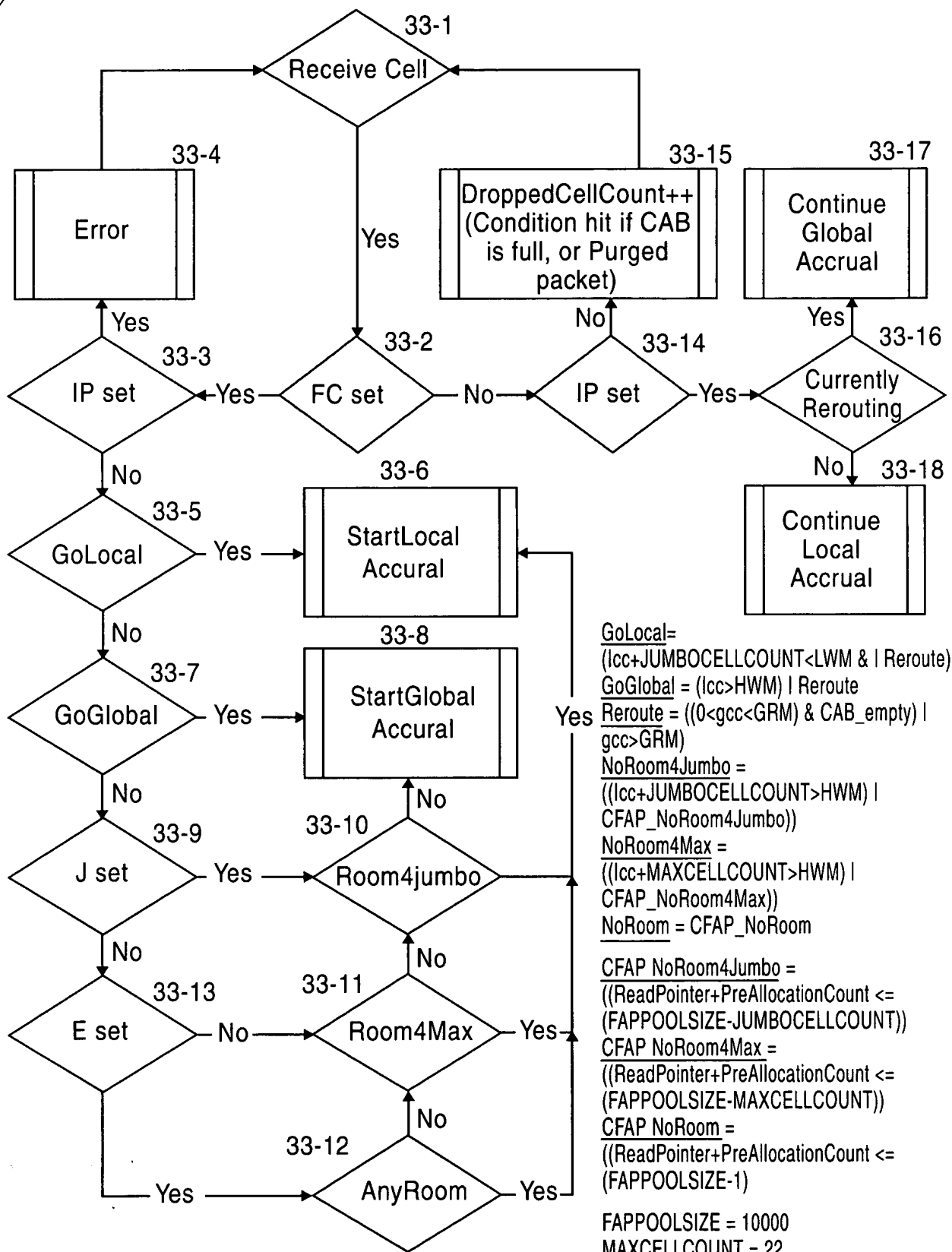


Fig.33

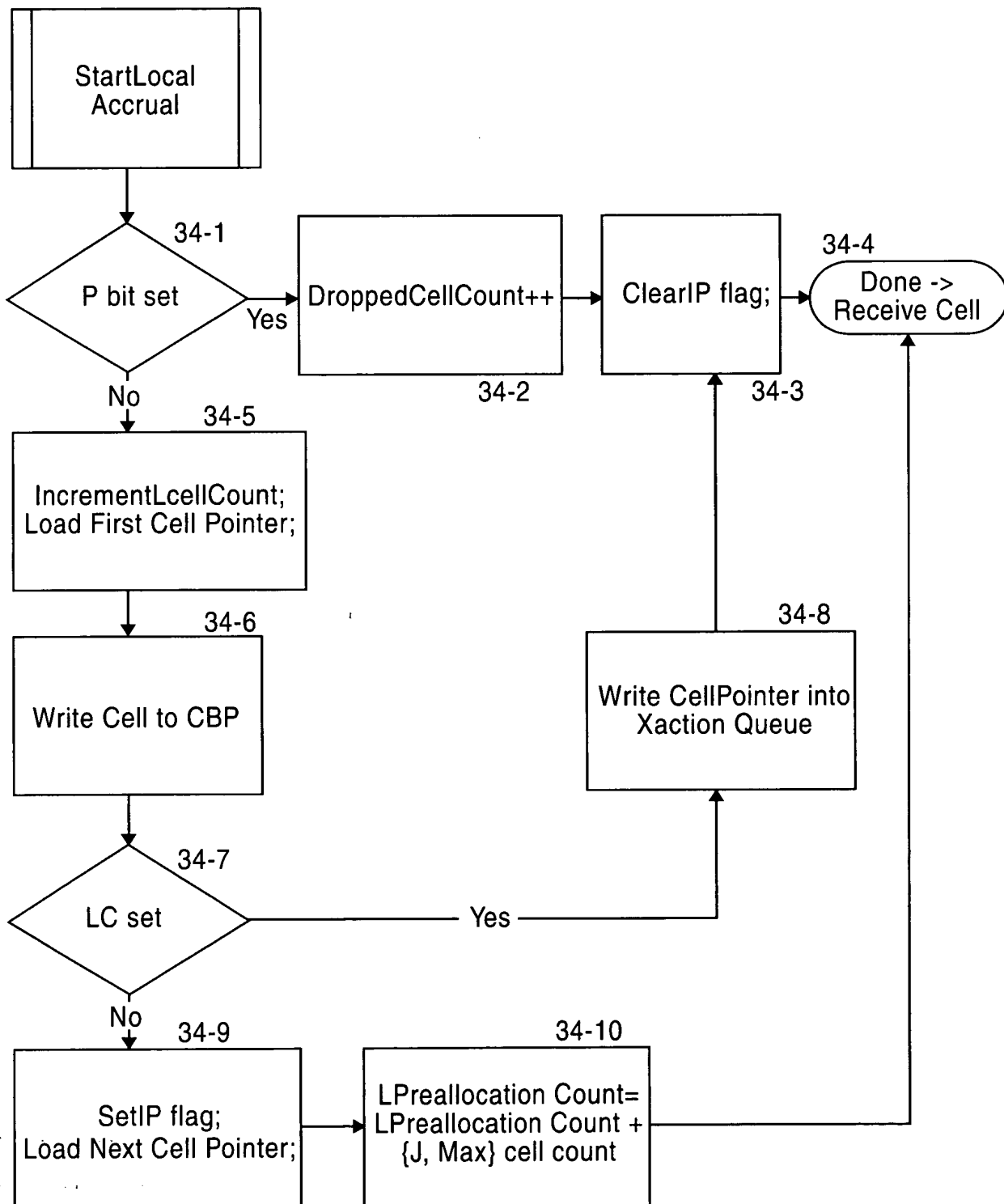
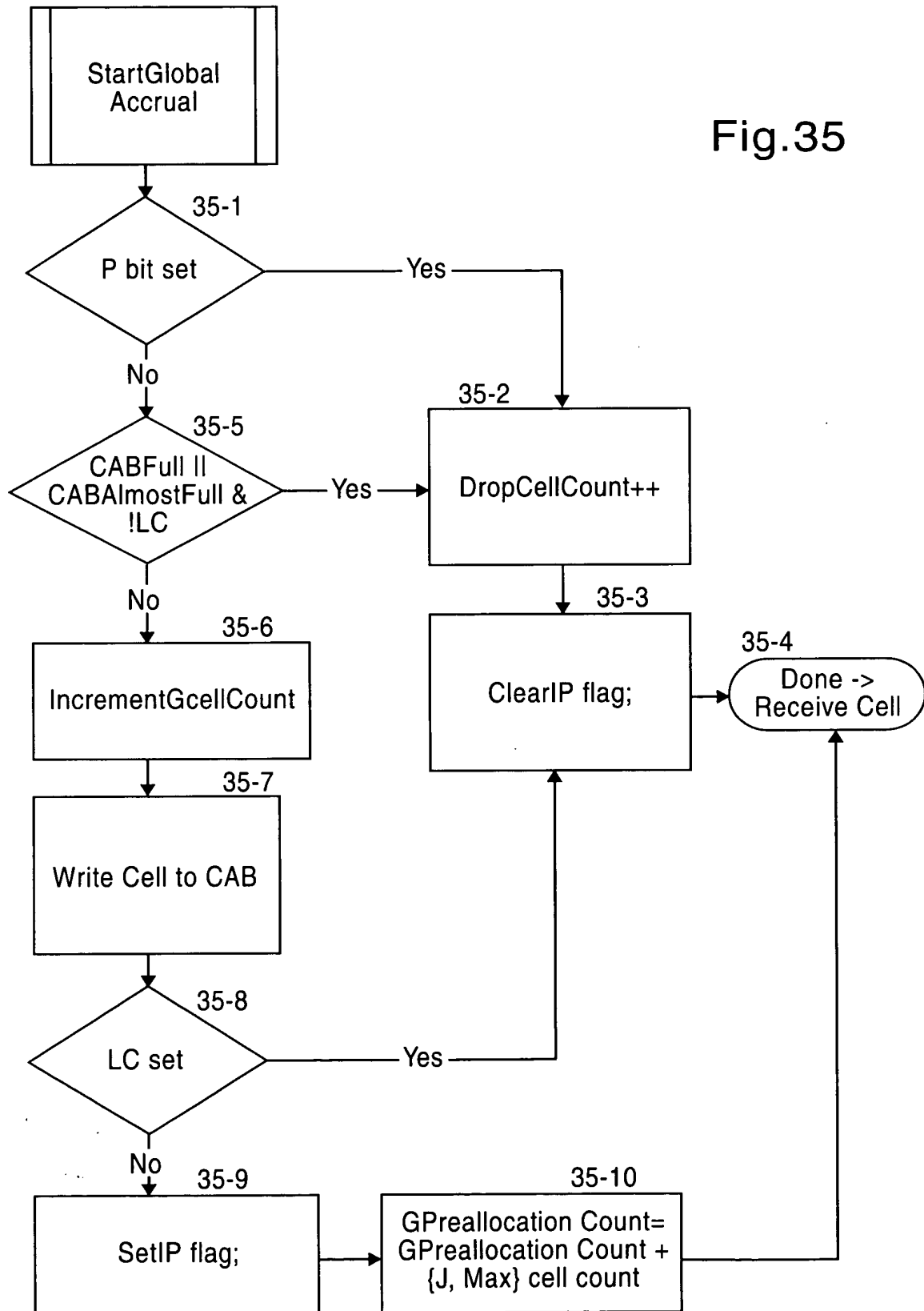


Fig.34



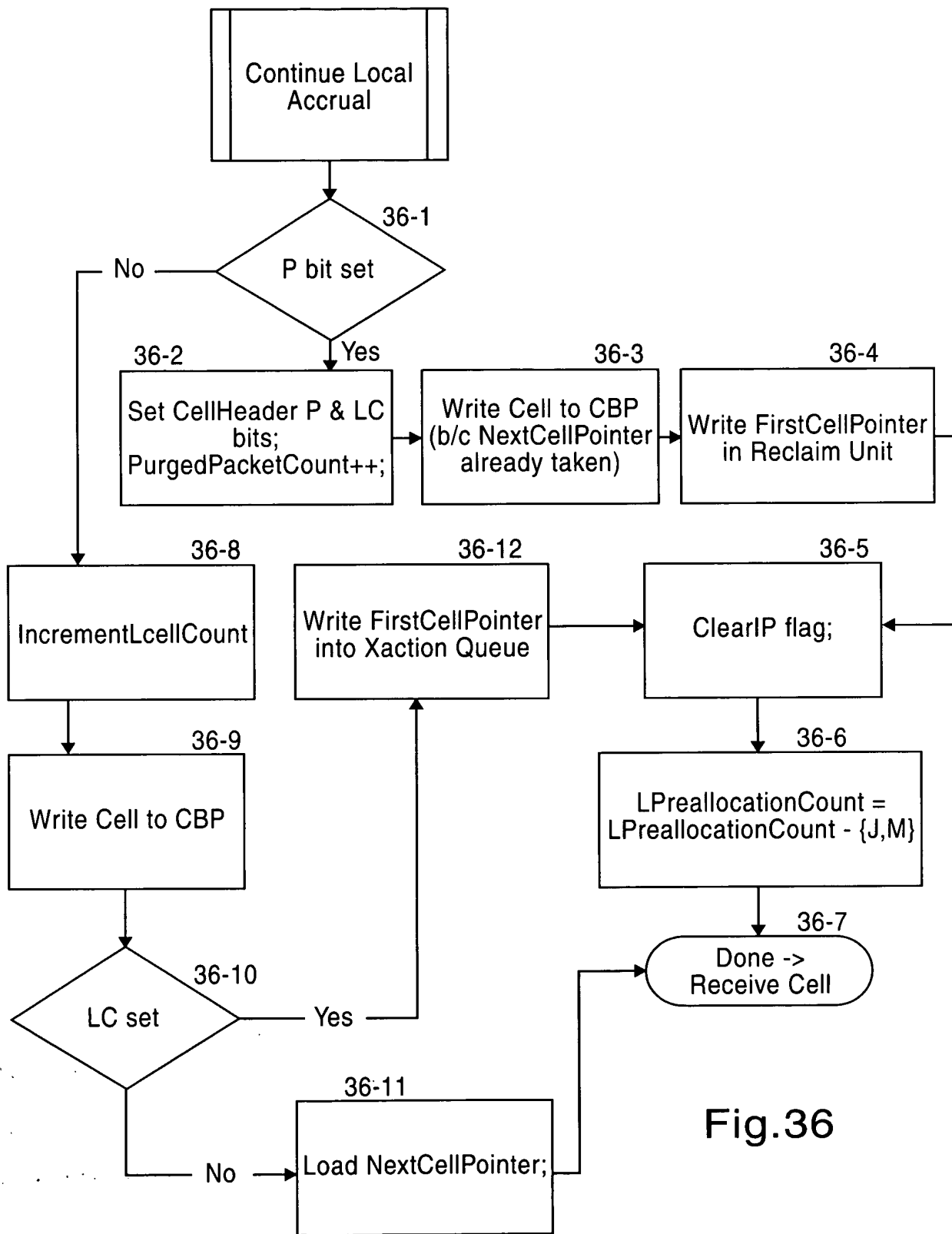


Fig.36

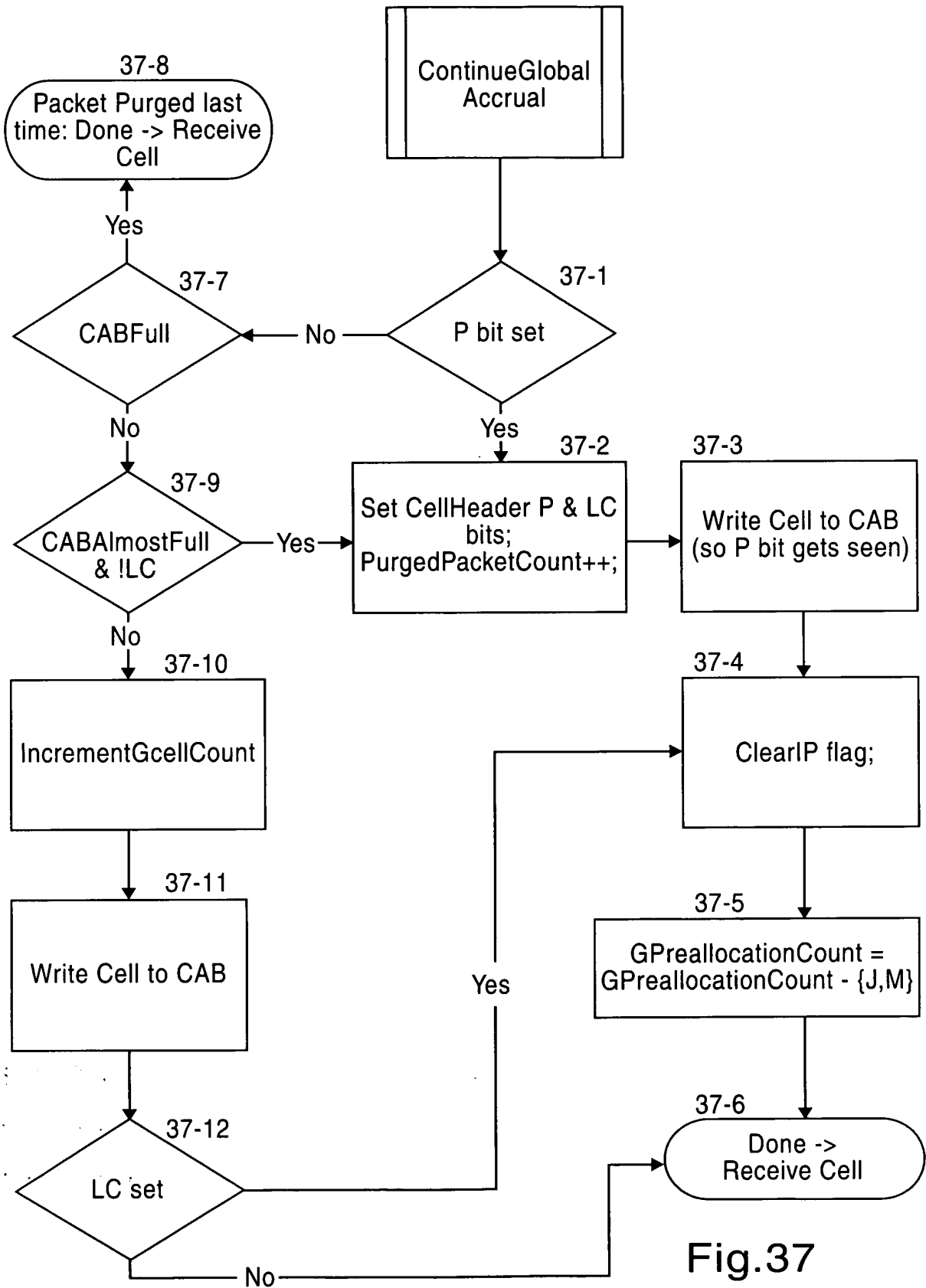


Fig.37

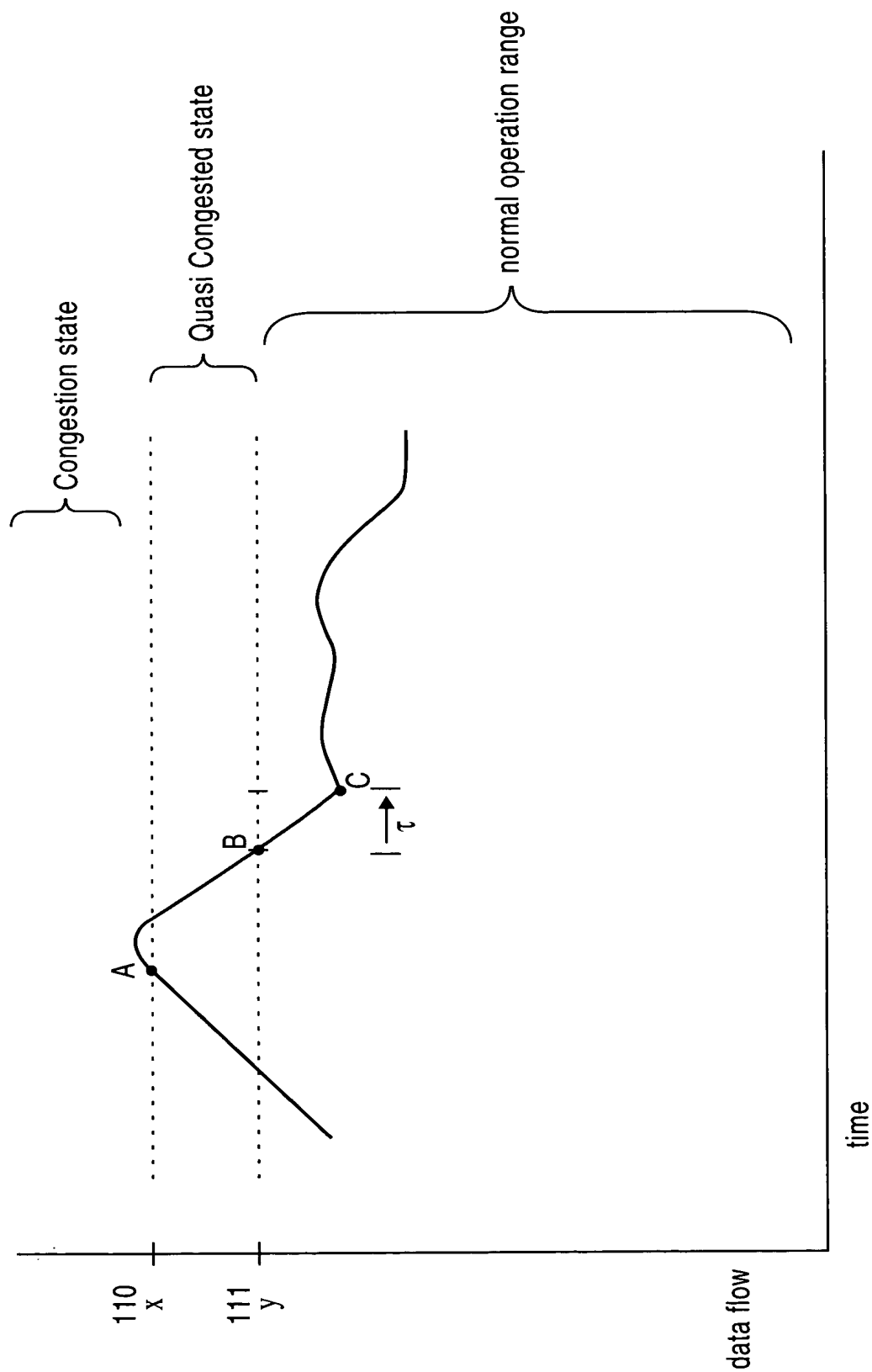


Fig.38



Fig.39

